We claimed:

1. A stacked package formed by stacking a plurality of semiconductor device packages, each package comprising:

a plurality of leads each including inner leads having a predetermined thickness and connection terminals having a thickness less than said predetermined thickness, said inner leads arranged along sides of a chip receiving area, said terminal ends lying adjacent to the chip receiving area;

a semiconductor chip located in the chip receiving area and being electrically connected to the connection terminals; and

a package body encapsulating the semiconductor chip, the inner leads, and the connection terminals, said package body having a thickness such that an upper and a lower surface of the inner leads is exposed, wherein each of the packages is stacked on another package by electrically connecting the exposed upper and lower surfaces of the inner leads with each other.

2. The stacked package of claim 1, wherein a lowermost package further comprises a plurality of outer leads integrated with the inner leads, said outer leads protruding from the package body.

3. The stacked package of claim 1, wherein the connection terminals are formed by etching a surface of the terminal ends of the inner leads.

4. The stacked package of claim 3, wherein the semiconductor chip is electrically connected to the connection terminals of the inner leads by a metal wire and a depth of the etching is greater than a wire loop height so that the metal wire is embedded by the package body.

5. The stacked package of claim 4, wherein the metal wire is wedge-bonded to the semiconductor chip and the connection terminals of the inner leads, respectively.

6. The stacked package of claim 1, wherein the semiconductor chip is electrically connected to the connection terminals of the inner leads by metal bumps.

7. The stacked package of claim 1, wherein the exposed upper and lower surfaces of the inner leads are plated with a Sn-Pb alloy.

8. The stacked package of claim 2, wherein the surfaces of the outer leads are plated with a Sn-Pb alloy.

9. A method for manufacturing stacked packages by stacking a plurality of semiconductor device packages, said method comprising:

preparing lead frames, each lead frame including a chip receiving cavity, a plurality of inner leads having a thickness, said inner leads arranged along sides of the chip receiving cavity, a plurality of connection terminals having a thickness less than that of the inner leads, each connection terminal being formed on a terminal end of the inner lead, said terminal end lying adjacent to the chip receiving cavity, a plurality of outer leads integrated with the inner leads, dam bars formed perpendicular to the inner and the outer leads in order to partition leads into the inner and the outer leads, and a side frame supporting the outer leads, the dam bars, and the tie bars;

supporting a semiconductor chip having electrode pads in the chip receiving cavity;

connecting the semiconductor chip to the connection terminals;

forming a package body by encapsulating the semiconductor chip, the inner leads, the connection terminals, and electrical connection parts

between the semiconductor chip and the connection terminals and limiting a thickness of the package body by an amount which is sufficient to avoid covering the upper and lower surfaces of the inner leads;

removing the dam bars from the side frame;

separating packages from the lead frame; and

forming a stacked package by stacking a plurality of the packages, wherein each of the packages is affixed to an adjacent package by electrically connecting the exposed upper and lower surfaces of the inner leads.

10. The method of claim 9, wherein the connection terminals are formed by a surface of the terminal ends of the inner leads.

11. The method of claim 10, wherein said connecting of the semiconductor chip to the connection terminals comprises electrically connecting the semiconductor chip to the connection terminals of the inner leads by a metal wire, and a depth of etching is greater than a wire loop height so that the metal wire is embedded by the package body.

12. The method of claim 11, wherein in said connecting the semiconductor chip to the connection terminals, the metal wire is wedge-bonded to the semiconductor chip and the connection terminals of the inner leads.

13. The method of claim 9, wherein said connecting the semiconductor chip to the connection terminals comprises:

forming a metal ball on each of electrode pads of the chip; and

electrically connecting the metal balls of the chip to the connection terminals by the reflow soldering.

14. The method of claim 9, wherein the lead frame comprises a lower lead frame and an upper lead frame, and further wherein a portion of said lower lead frame comprises the connection terminal.

15. The method of claim 9, wherein said separating the package from the lead frame comprises:

severing the outer leads from the side frame and bending the outer leads to be mounted on an external printed circuit board, wherein the semiconductor package is the lowermost package of the stacked package.

16. The method of claim 15, wherein the outer leads of the lowermost package are bent in a gull-wing shape.

17. The method of claim 9, wherein said separating the package from the lead frame comprises:

severing the inner leads from the outer leads, wherein the semiconductor package is stacked on the lowermost package of the stacked package.

18. The method of claim 9, further comprising plating the exposed upper and lower surfaces of the inner leads and the surfaces of the outer leads with a Sn-Pb alloy.

19. The method of claim 18, wherein in said forming the stacked package, the inner leads of one package are bonded to the inner leads of another package by the reflow soldering.

20. The method of claim 9, wherein in said forming the stacked package, the inner leads of one package are bonded to the inner leads of another

package by applying a solder paste on the exposed upper surfaces of the inner leads and reflow soldering the applied solder paste.

21. Semiconductor chip and package structure, said structure comprising:

semiconductor chip having a plurality of electrode pads;

a plurality of electrically conductive leads, each having an inner end and an outer end, the inner end of each lead being coupled to an associated electrode pad;

a housing encapsulating said semiconductor chip and a portion of each of said leads, said housing having an upper surface, a lower surface and a thickness, wherein a portion of said leads have a thickness sufficient to expose an upper surface and a lower surface of each lead at the upper and lower surfaces, respectively, of said housing.

22. The structure according to Claim 21, wherein the outer end of said leads terminate at a location beyond a perimeter of said housing.

23. The structure of Claim 21, wherein said leads are comprised of first and second electrically conductive members.

24. The structure of Claim 22, wherein said leads are comprised of first and second electrically conductive members.

25. The structure of Claim 21, wherein the inner ends of said leads have a thickness less than a thickness of the leads at a position displaced from the inner end.

26. The structure of Claim 22, wherein the inner ends of said leads have a thickness less than a thickness of the leads at a position displaced from the inner ends.

27. The structure of Claim 23, wherein an inner end of one of said first and second electrically conductive members extends more closely to an edge of said chip than the inner end of the other of the first and second electrically conductive members.

28. The structure of Claim 24, wherein an inner end of one of said first and second electrically conductive members extends more closely to an edge of said chip than the inner end of the other of the first and second electrically conductive members.